RESISTORS • CAPACITORS • COILS • DELAY LINES

Delay Line Application Manual

Engr Report No. R-45

FOREWARD

Delay line products are a rather sophisticated and complex technology. Unfortunately, it seems that all industry literature addressing delay lines to date, including RCD's, has been equally complicated and technical.

This application manual has been developed not only to assist Component Engineers, but also to aid Buyers, Quality personnel, and Distributor Product Specialists in the selection, handling, inspection, and general understanding of delay lines. We have tried to accomplish this in a user-friendly format, without sacrificing any engineering detail.

The manual is intended to be utilized in conjunction with RCD's Delay Line data sheets. The first section of this guide provides an overview and history of delay line products, of which our involvement stretches back nearly 50 years! The latter sections address a myriad of technical details, enough to exhaust even the most demanding engineer.

Table of Contents

Section 1: General Overview of Delay Lines

Section 2: Technical Aspects of Passive Delay Lines

Table of Contents (continued)

Table of Contents (continued)

What is a Delay Line?

A delay line is a component that will briefly delay a signal in a circuit, i.e. it takes an input signal and reproduces the same signal at its output but delays it a precise period of time. The simplest and perhaps oldest delay line is a piece of coaxial cable. The longer the cable, the longer the time required for the signal to travel from input to output. Delay times over a few nanoseconds (billionths of a second) would of course require unreasonable lengths of cable, so the use of an active or passive delay line is much more economical and accurate, involving much smaller amounts of PCB real estate.

RCD Delay Line History – Over Fifty Years of Expertise

Delay lines were developed in the late 1940's for the television industry, and were primarily of distributed constant design which were bulky, expensive, and of limited performance. The vacuum-tube circuitry of the time typically required delay times in microseconds.

RCD's Chairman, Louis J. Arcidy, was actively involved in the pioneering and development of resistors, coils, and delay line products for nearly twenty years before founding RCD Components in 1973.

With the emergence of transistors and later the integrated circuit, response speeds were considerably increased. RCD's delay line development throughout the 1970's and 80's was driven by the need for faster delay lines primarily for the computer and peripheral markets.

More recently, the rapid increase of data transmission networks and high frequency chipsets, have resulted in the need for crucial and infinitesimal timing control. Today, most delay times are measured in the nanosecond and picosecond ranges, although some applications still require longer (microsecond) delays. RCD offers the industry's widest range of delay times, ranging from 20pS (2×10^{-13} seconds) to 20μS (2×10^{-5}).

RCD has developed a wide variety of specialty delay line products specifically for telecom circuits, precision medical instrumentation, aerospace, military, and a host of other applications. A specialty thin film design enables passive delay lines at operating frequencies up to 4GHz. Customized and specialty delay lines are a very vital and rapidly growing segment of RCD's business. Over half of RCD's delay line business is attributable to custom products.

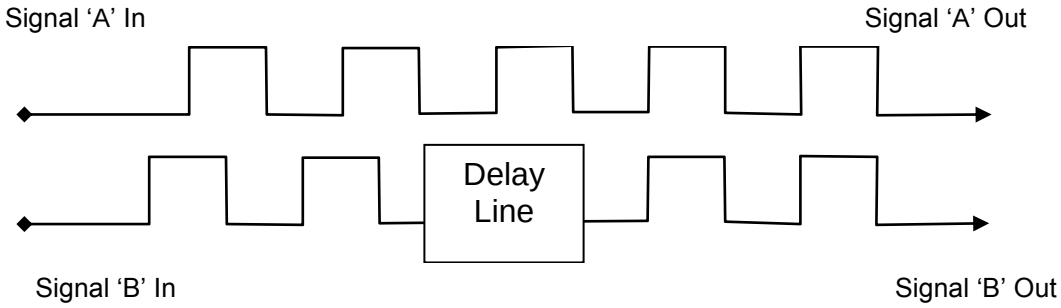
RCD continues to be a leader in the industry with innovative new designs, and provides a complete range of passive and active delay lines including various DIP, SIP, and surface mount packages.

Delay Line Function

The basic function of a delay line is to introduce a time delay in the transmission of an electrical signal. This function is utilized in a variety of ways, primarily for circuit timing, signal conditioning, and power conversion, enabling maximum system performance in memory management, clock timing, bus management, pulse shaping, phase shifting, phase inversion, etc.

An ideal delay line would delay a signal without distorting or altering the signal, i.e. it would "store" the exact signal information, whether analog or digital, while the signal is in the process of being delayed. Since nothing is perfect, electronic amplification is required to compensate for inevitable losses. The result is an economical information-storage device that is applicable to a wide variety of applications.

The most common application for delay lines is to achieve precise control of signal timing. Many circuits require that two signals arrive at a particular junction at the same time. Differences in conductor trace paths, interconnects, circuitry, etc., can result in one signal arriving sooner than the other. A delay line is utilized to "stall" one signal thereby enabling both signals to synchronize.



A specific example is in the magnetic drive industry in which delay lines are utilized to offset the shift caused by the magnetic properties of the storage medium. This enables the data to be properly synchronized thereby eliminating storage errors that would otherwise result.

Delay lines are also frequently utilized in circuits with clock oscillators to produce another phase of the clock signal. Delay lines can also multiply the functions of the clock signal.

Types of Delay Lines

Time delays can be achieved either by various electro-mechanical means, such as ultrasonic delay lines, or by purely electromagnetic means (passive lumped

constant, distributed constant, and active delay lines). RCD offers all types of delay lines except ultrasonic models.

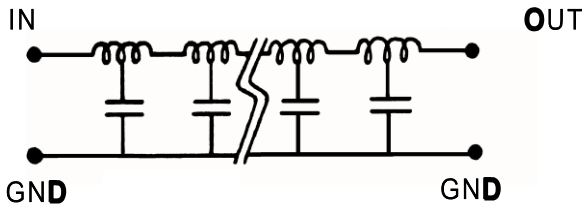
Ultrasonic Delay Lines

Ultrasonic delay lines (also referred to as Acoustic, Glass, and Quartz delay lines) convert electrical energy into mechanical energy via sound waves. The frequency of the waveform is much slower than electrical energy thereby enabling long delay times. The delay is equal to the time required for the acoustic wave to travel through the transmission medium (glass, quartz, or metal) from input to output transducer. Ultrasonic delay lines are costly and rather large modules primarily intended for military applications, such as radar and sonar signal processing, not for PCB applications. RCD does not manufacture ultrasonic delay lines.

Electromagnetic Delay Lines

Electromagnetic models delay signals via a network of inductors and capacitors, selected to achieve a particular delay time, and are designed primarily for PCB use. There are two categories of electromagnetic delay lines - Active and Passive. Active models include traditional hybrid IC models and newer all-silicon models. Passive models include Lumped Constant and Distributed Constant. Distributed constant delay lines are constructed by winding the inductor coil onto a metallic core. The capacitance is then distributed along the inductor windings. Distributed constant delay lines are rarely utilized anymore due to high cost and relatively low bandwidth, and as such are not manufactured by RCD.

Passive Delay Lines



Passive delay lines are specialty low pass L/C filters which delay or shift the phase of a signal by a predetermined amount of time or degrees. Inductors and capacitors are "lumped" into networks with inductors shunted by capacitors, thus the Lumped Constant designation. Schematically, the inductive and capacitive elements may be depicted as shown above.

Delay times are altered by changing the values of L (inductance) and C (capacitance). Passive delay lines are able to pass any shape signal, either analog or digital (within inherent bandwidth limitations), but are generally utilized in analog applications where signals are typically a sinewave type. Passive delay lines operate on the power of the input signal alone. They do not amplify or create

energy. Passive devices need to be properly terminated to match the characteristic impedance during operation. RCD offers a wide range of passive delay lines in SIP, DIP, and surface mount packages. Tapped units are available with 5, 10, or 20 taps.

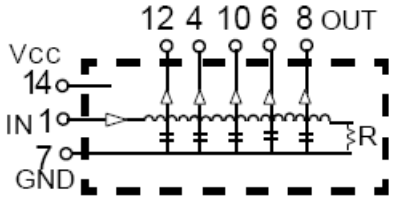
Active Delay Lines

Active delay lines hold the same properties as passive delay lines but are specifically designed for digital circuits (i.e. digital pulses generated by a specific logic family). Active delay lines are internally buffered with a specific logic family thereby enabling a "plug and play" approach, i.e. no special termination or circuitry considerations.

RCD offers active delay lines in SIP, DIP, and surface mount styles in all standard logic families including...

- Schottky TTL (Transistor-Transistor Logic)
- LSTTL (Low Power Schottky TTL)
- ALS (Advanced Low Power Schottky)
- FAST® (Fairchild Advanced Schottky TTL)
- ASTTL (Advanced Schottky)
- 10K ECL (Emitter Coupled Logic)
- 10KH ECL
- 100K ECL
- HCMOS (High Speed CMOS)
- FACT® (Fairchild Advanced CMOS)

A typical multi-tapped Active delay line circuit schematic is given below...



A1405 Schematic

Cost Considerations

When specifying a delay line, circuit designers should keep in mind that there's often more than one way to meet a given requirement. An overspecified parameter may substantially increase cost.

The prime parameters that must be considered in specifying a delay line are:

1. Delay Time
2. Rise Time
3. Attenuation
4, Impedance
5. Distortion
6. Temperature Coefficient
7. Operating Temperature Range
8. Package and Schematic Design
9. High-Reliability Screening

Of these parameters, rise time, delay time and attenuation are closely related and have a large effect on the complexity and cost of a delay line.

Delay Time

Passive delay times from 20pS to 20μS are available from RCD to meet specific requirements. Costs increase substantially above 2μS range due to the large number of L/C sections and specialty materials required. Active delays are available from 5nS to 1000nS. Delay time and tap tolerances are typically specified as ±5% or ±10%, but are available as tight as ±1% to ±2% in some products at a price premium.

RCD Components also provides delay line packages consisting of several increments with one common ground, and the input/output taps of each increment brought out for external connection.

Rise Time

The absolute values of the rise time and delay time parameters are generally not critical (rise times are normally specified as a maximum). The Delay Time (Td) to Rise Time (Tr) ratio is probably the most important factor in determining the cost of a passive delay line since it determines the number of L/C sections required.

The increase in the number of sections can grow at a rate of 2 to 4 times the Td:Tr ratio. And, as the sections increase, their individual section efficiency decreases. To compensate for this, more complex section designs are required and consequently the cost increases.

Since input pulse width may considerably affect the design of a delay line, this parameter should always be given. As a rule of thumb, the width of the input pulse should be at least two times the required delay line rise time to avoid added attenuation or special design. Normally, rise time measurements are made from 10% to 90% of the leading edge of the delayed pulse; however, in some applications, the rise time between two intermediate amplitude levels on the leading edge is more important than the total rise time and the total amplitude.

When this is the case it should be specified.

Attenuation
Attenuations typically are from 0.2 to 3db depending on delay and compactness of the line. Special core materials are available for extremely low attenuation, but often RCD can lower the attenuation simply by increasing the case size slightly, which has only a minor effect on cost. Attenuation is generally specified as a maximum.

Generally, as the attenuation in a delay line is decreased, the complexity and cost increase. With input pulse characteristics which obey our rule of thumb, the attenuation of the output pulse is dependent mainly on the individual inductor design. The maximum input pulse amplitude will be limited by the dielectric strength of the capacitors or the saturation point of the inductors. The problem of inductor saturation, however, occurs more often with relatively long delay lines. A more serious consideration may be the size of the overall package since lower voltage capacitors can be obtained in smaller sizes than the higher voltage capacitors. Typical working voltages are from 50 to 500 VDC. Working voltage is specified as a minimum.

Impedance
RCD produces delay lines with impedances ranging from 50 to 2000 ohms. Impedances from 20 to 10,000 ohms are available. The easiest and most straightforward impedance parameters are between 50 and 500 ohms. Typical tolerance is ±10%.

Distortion
Distortions typically run 5% to10% and in certain instances 15 to 20%. RCD can supply delay lines with distortions as low as 2%. It should be remembered, that distortions are input rise time dependent, i.e. a delay line which exhibits a distortion of ±10% with a 3ns input rise time may only show +-5% with a 10 ns input rise time. If distortion is to be reduced on a given line, cost will increase.

Temperature Coefficient
Another major factor affecting delay line costs is the temperature coefficient (TC). A low TC indicates that the delay time will not vary much with respect to temperature. The more economical design is achieved when TC for the delay line is ±100 parts per million (0.01%/°C) or higher. Specifications calling for TC's of ±50 ppm or lower require special materials and testing, consequently, the cost rises significantly.

Operating Temperature Range
The standard continuous operating temperature range for active and passive

delay lines is 0°C to +70°C. RCD also offers an industrial temperature range of -40 to +85°C (request Option "39") and a military-grade temperature range of -55°C to +125°C (request Option "ER"). The cost adder for the latter is rather significant.

Storage temperatures should be specified separately from operating temperatures, since the delay line need not perform at storage extremes.

Package and Schematic Design

The physical configuration of a delay line is almost the same as its schematic configuration. To achieve lowest cost, the package design and pin designation should correspond to the basic internal layout of the delay line circuit board design. If the printed circuit board design establishes a tangled pattern for terminal locations, the package complexity may increase substantially and drive up costs. Passive Dip delay lines are available in a variety of schematics in addition to those listed in RCD's data sheets.

Sip and Dip packages are approximately the same price although Dip's are more readily available since they are more popular. Surface mount packages are available in almost all models, typically at a 25% price premium.

High Reliability Screening

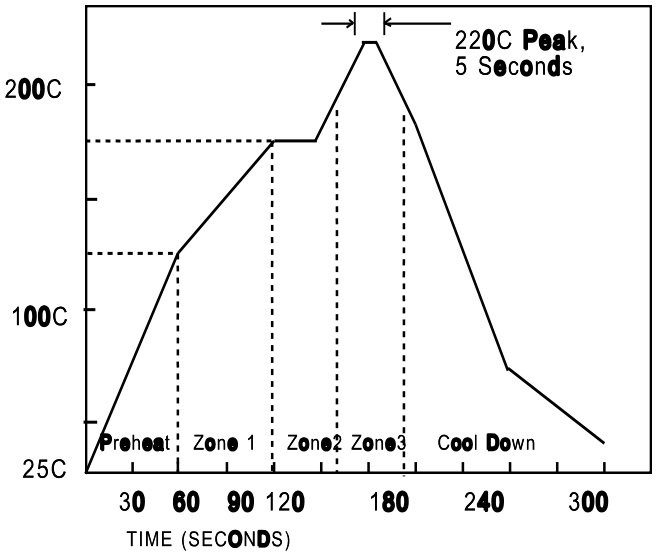
RCD offers full environmental screening for demanding requirements such as military, medical, and aerospace. Screening may include a variety of environmental parameters on 100% or sample basis as specified by customers including...

- 100% Pre-cap Visual Inspection
- Delay Time at Elevated Temp
- Delay Time at Low Temperature
- Temperature Coefficient
- Insulation Resistance
- Life/Burn-In
- Low Temperature Operation
- Vibration
- Dielectric Withstanding Voltage
- Impedance
- Flammability
- 100% Delay Time testing
- Thermal Shock
- Voltage Attenuation
- Distortion
- Rise Time
- DC Resistance
- Temperature Cycling
- Moisture Resistance
- Solderability
- Terminal Strength
- Resistance to Solvents
- X-Ray Analysis

Surface Mount Soldering Guide

Solder methods for RCD's SM active and passive delay lines are Infra Red and Vapor Phase reflow. A recommended temperature profile for the IR reflow process

follows. Peak temperature not to exceed 220°C, and 45 seconds max above 185°C. Gradual ramp-up and cooling is recommended.



TECHNICAL ASPECTS OF PASSIVE DELAY LINES

Delay and Impedance (Td & Zo)

The delay time and impedance of a delay line may be expressed as:

$Zo(ohms) = (Lt/Ct)^{1/2}$ $Td\ (nS) = (Lt \times Ct)^{1/2}$

Ct = total network capacitance in pF
Lt = total network inductance in μH
Td = time delay in nS
Zo = characteristic impedance in ohms

As can be seen, the total capacitance and inductance for a particular delay line are related to the total delay and impedance specified. Higher impedance delay lines have lower capacitive sections and higher inductive sections, and vice versa for low impedance delay lines.

Rise Time (Tr)

The rise time of a delay line may be expressed as:

$$Tr = (Tro^2 - Tri)^{1/2}$$

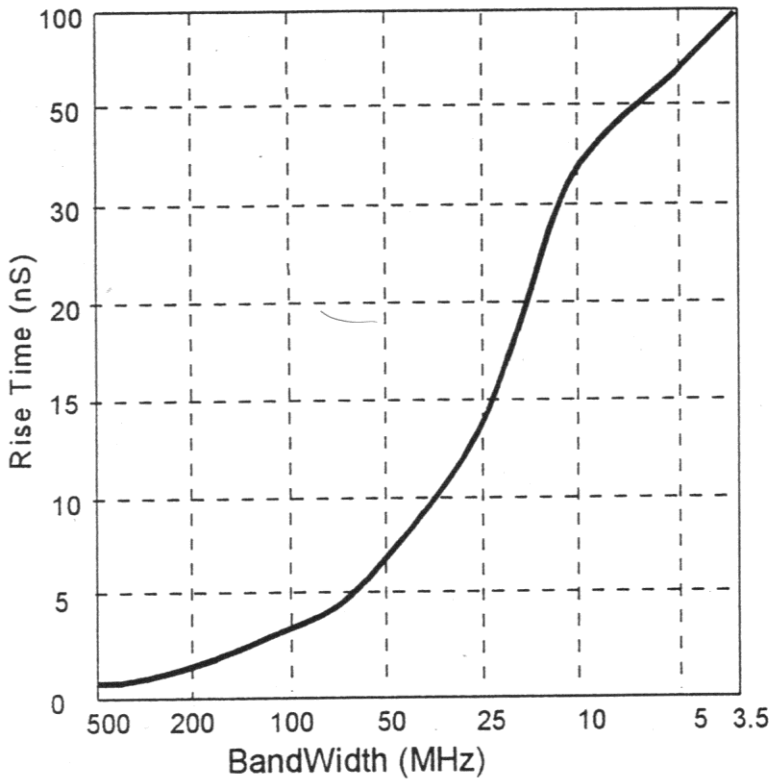
Tr = Network Rise Time
Tri = Input Rise Time
Tro = Output Rise Time

The bandwidth of the delay line is related to rise time (assuming a linear phase response) and is expressed as:

BW(MHz) ≅ .35 ÷Tr (uS)
Tr (uS) ≅ .35 ÷ BW (Mhz)

BW = cutoff frequency of the delay line in Mhz at -3 db point

Bandwidth to Rise Time Chart

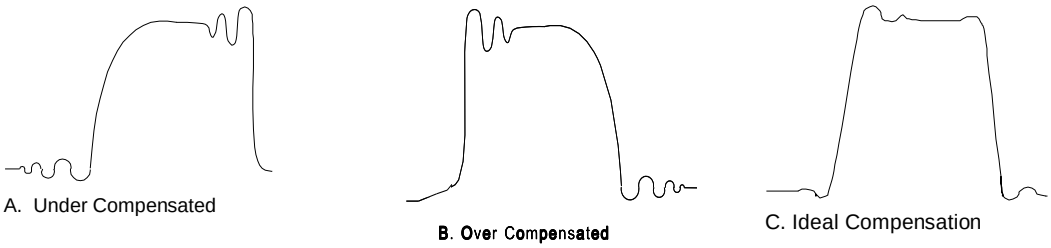


Frequency Response and Phase Compensation

Frequency response is a function of the number of sections into which Lt and Ct are divided. A larger number of sections will reduce L & C of each section thereby increasing the overall frequency response. RCD offers delay lines with frequency response up to 4GHz. Since most delay line inputs are composed of varying harmonics, it is desirable for a delay line to have linear phase response to ensure that all frequency components (harmonics) are delayed equally. Mismatches will result in pulse shape distortion.

If the higher frequencies of the incoming pulse are delayed to a greater extent than the lower frequencies, then the output pulse of the delay line will appear as per illustration "A". If the higher frequencies are delayed less than the lower ones, than the output pulse will appear as per illustration "B". Ideal compensation

will result in output pulse per illustration "C". Proper phase compensation is complex and depends in part on the internal coupling of the magnetic structure. The frequency response of a delay line affects its ability to approach the rise time of the input pulse to be delayed. Generally however, the concern is the pulse shape rather than frequency. Therefore, frequency response is not considered as such, but is accounted for in rise time of the delay line.



Quality Factor (Figure of Merit)

The delay time to rise time ratio (Td/Tr) is the quality factor or figure of merit of a delay line. The amount of inductance and capacitance assigned to each section of a delay is dependent on this ratio.

Attenuation

The total voltage attenuation in a delay line may be the effect of several separate sources of loss:

1. Internal DC resistance of the delay line
2, Ground plane losses
3. Tap Loading
4. Mismatched terminations
5. Pulse width limitations

Internal D.C. Resistance

The DC resistance is attributable primarily to the inductor windings. The resulting attenuation from this loss source may be expressed as:

Attenuation (%)=1- [Zo/(DCR + Zo)]

Zo = Characteristic impedance of the delay line in ohms
DCR = Total DC Resistance (Input to Output) in ohms

Ground Plane Losses

Ground planes to the delay line should be as massive as feasible, and preferably positioned beneath the delay line package between the rows of leads. All ground terminals provided on the delay line should be used.

Tap Loading of Passive Delay Lines

Delay lines with higher impedance values have lower capacitive sections which can result in problems for tapped units, particularly when the total delay time is below 40nS. A PC board trace can load a tap with 3pF to 10pF which will increase the delay time, rise time, distortion, and attenuation. Therefore, it is recommended that circuit designers minimize trace lengths to the delay line.

The Attenuation due to a tap load may be expressed as:

Attenuation = Ei [1/(1 + Zo/2R)] - 1

Ei = Voltage at input
Zo = Characteristic impedance
R =Load of Tap

Tap loading should be minimized. Tap terminating impedances should be at least 10 times the characteristic impedance of the delay line. Otherwise noticeable reflections will appear at the input of the line and the output pulse will be more attenuated. If resulting reflections and attenuation are not detrimental to circuit operation, lower terminations may be used. The output pulse shape is not affected by lower tap terminating impedances. If a tap is connected to a capacitive load, reflections will result, if the load is a significant portion (i.e. >10% to 15%of the section capacity of the line). If loads are above this level, it is recommended to connect a buffer between the tap and load. As an alternative, RCD can customize a construction suited to the particular application, providing that tap spacing is held so that each tap will fall on a capacitor and the capacitive load does not exceed the value of the section capacitor.

Mismatched Terminations

Voltage losses or gain due to impedance mismatch at the output of a delay line may be expressed as:

Et = Ei/[(Zo/2xRt) + 1/2], or

Er = Ei x [1/{(Zo/2xRt) + 1/2} - 1]

Et = Voltage at termination
Ei = Voltage at Input
Zo = Characteristic impedance of the delay line
Rt = Terminating value of resistor
Er = Voltage reflected at input

The output of the delay line should be terminated in its characteristic impedance

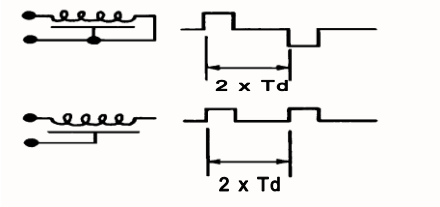
using a non-inductive resistor, to prevent the pulse, traveling down the line, from being partially reflected back to the input.

In general, reflections such as termination mismatch are undesirable since this will result in distortion and added attenuation in the input and output pulses. However, terminating a delay line in an impedance other than its characteristic impedance can be used to advantage in certain applications. These are met by reflected delay lines.

Pulse Width Limitations

The width of the input pulse should be at least two times the the required rise time as mentioned previously in this manual. Problems can occur with narrow pulse widths. For instance if the pulse width is the same as the rise time, there would be inadequate time for the leading edge to attain full amplitude, thereby causing additional attenuation at the output. If the input pulse width is less than the rise time, the output pulse will be stretched such that the width is wider than the input at the 50% level. Design consideration should be given to avoid this situation when converting logic edges to output pulses, especially where falling edges are involved.

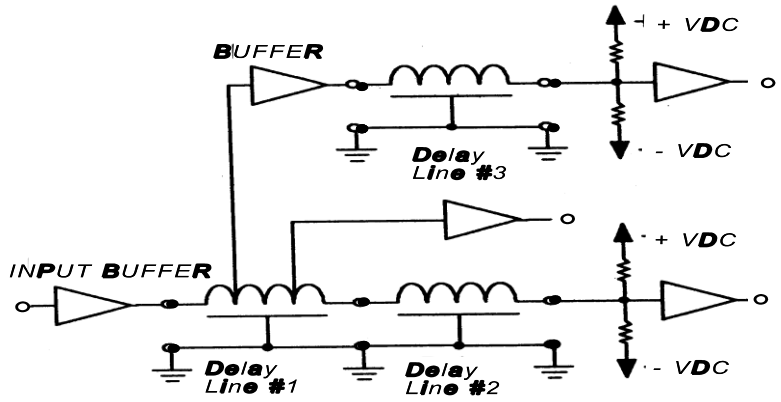
Reflected Delay Lines



A reflected delay line is terminated in either an open or a short circuit. Viewed from the input terminals the pulses will appear as illustrated. The amplitude of these reflections will be 100% of the input voltage less the regular delay line attenuation for both directions. Since the total delay has increased to twice that of a one way delay line, a reduction in the number of sections can be realized for a given Td/Tr.

Combining Delay Lines in Series

In order to achieve longer delay times, or a particular delay and rise time combination not covered by standard products, passive delay lines may be connected in series from input to output (also known as "cascading"). When cascaded, delay lines do not need to be individually terminated if of the same characteristic impedance value. A typical Thevenin style series connection schematic is depicted below...



It is recommended that customers evaluate prototypes in their actual circuits, especially if cascading more than a few units, to ensure that the desired characteristics are optimized.

If utilizing delay lines of unequal delay times, it is recommended that the longer delay times precede the shorter ones in the series connection. The output signal's rise and fall times increase with cascading, therefore it is recommended that wider input pulses be utilized or preferably that the cascaded units be rebuffered. Rebuffering will greatly reduce attenuation, reflections, distortion and rise time loss.

The approximate Output rise time of a group of delay lines connected in series can be calculated as follows...

$$\text{Total Rise Time} = (Tr_{in}^2 + Tr_1^2 + Tr_2^2 + \ldots Tr_n^2)^{1/2}$$

Tr_{in} = Rise time of the input signal
Tr_n = Rise time of each delay line

Voltage Capability

Passive delay lines are not voltage sensitive devices, however voltages can cause inductor saturation in some instances, particularly with relatively long delay times. High voltage capacitors are available on a custom basis although this often requires an increase in package size and price. Working voltage is 50V or above on most models, although typically not encountered in today's low voltage circuits.

Another voltage rating is the Dielectric Withstanding Voltage capability, otherwise known as "dielectric strength" or "Hi-pot". The DWV is the voltage level that the package insulation is capable of withstanding when voltage is applied

between the terminals and the insulation. RCD delay lines are typically rated for dielectric strengths of 100V but are available up to 1KV on special order.

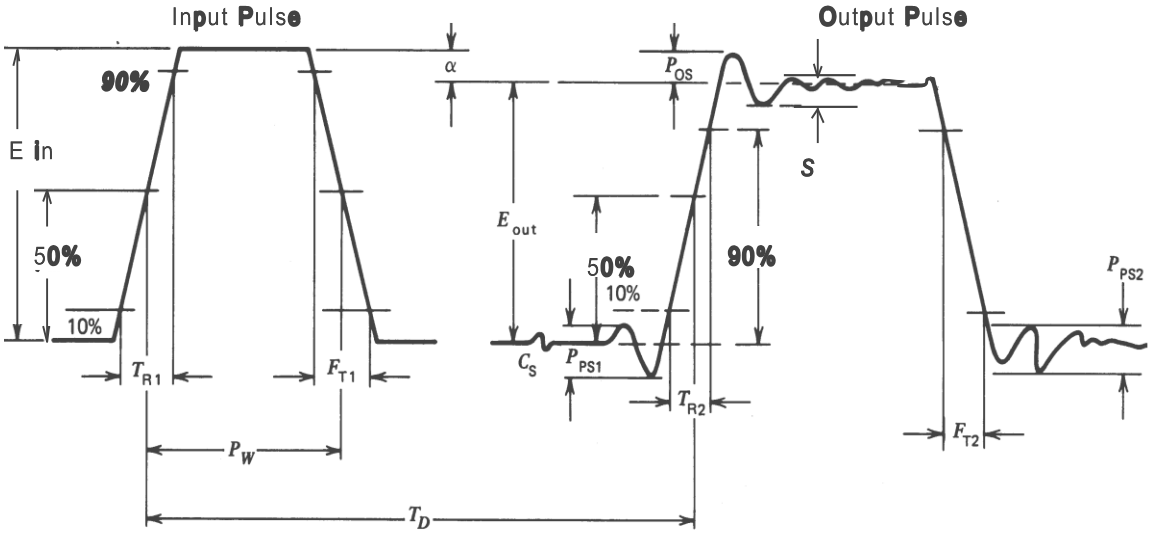
Duty Cycle

The input pulse repetition rate generally has no effect on the performance of passive delay lines, unless the duty cycle becomes so high that the distortion of a pulse is added to the reflections of the previous pulse. This interaction is reduced or eliminated when the pulse width of a pulse train is longer than the total delay of the delay line, and the duty cycle is less than 25%.

ESD Characteristics of Passive Delay Lines

RCD's passive delay lines are not ESD (Electro-Static Discharge) sensitive and therefore do not require special handling or storage. Active delay lines are ESD sensitive (refer to active delay line section).

PASSIVE DELAY LINE DEFINITIONS



Attenuation (α) The difference in voltage between the input and output pulses

Crosstalk: The amount of input pulse reflected directly into the output pulse

DC Resistance (DCR) The D.C. resistance in ohms (Ω) measured from the input to the output of a delay line

Delay Time (T_D) The time duration between the 50% point on the leading edge of the input pulse and the 50% point on the leading edge of the output pulse

Dispersion: The variation of time delay due to frequency

Feedthrough Leakage: A spurious signal which arrives at the output by electrical coupling

Frequency Response: A representation of the insertion loss or the voltage attenuation as a function of frequency

Impedance (Z_O) The value of terminating impedance which provides minimum reflection back to the input

Input Fall Time (F_{T1}) The time duration between the 90 and 10% points on the decreasing edge of the input pulse

Input Rise Time (T_{R1}) The time duration between the 10 and 90% points on the increasing edge of the input pulse

Input Voltage (E_{In}) The amplitude of the input pulse

Insertion Loss: The ratio of the power delivered to that part of the system following the delay line, before the insertion of the delay line, to the power delivered to the same part of the system after insertion of the delay line

Leading Edge: The portion of the pulse which rises from zero to peak amplitude

Output Fall Time (F_{T2}) The time duration between the 90 and 10% points on the decreasing edge of the output pulse

Output Rise Time (T_{R2}) The time duration between the 10 and 90% points on the increasing edge of the output pulse

Output Voltage (E_{OUT}) The amplitude of the output pulse

Postpulse Spurious (P_{PS2}) The output pulse excursions following the main pulse

Prepulse Spurious (P_{PS1}) The output pulse excursions prior to the main pulse

Pulse Distortion (S) The magnitude of the largest peak amplitude of all spurious responses in either a positive or negative direction occurring in the period after

the top of the leading edge of the output pulse and before two time delays

Pulse Overshoot (P_{OS}) The amplitude of the overshoot on the leading edge of the output pulse

Pulse Width (P_W) The time duration on the input pulse between the 50% point on the increasing edge and the 50% point on the decreasing edge

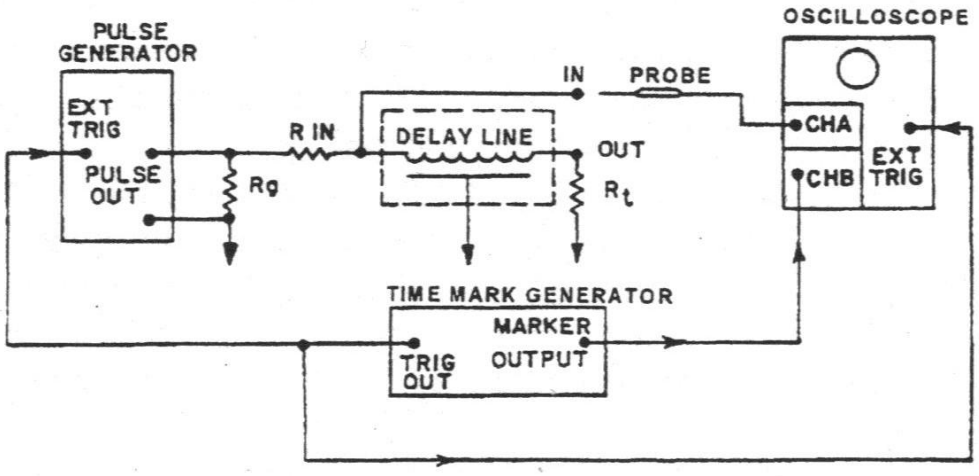
Spurious Level: The ratio of a spurious signal to the desired signal, expressed in decibals, measured at a specific frequency over a specified band of frequencies

Tapped Line: A delay line in which the total delay is divided into smaller sections and available at each output tap. Standard models are available with 5, 10, or 20 taps (customized models avail.). Consult Section 4, Delay Line Selection Chart.

Temperature Coefficient of Delay: The variation of delay with temperature measured in parts per million per °C (100ppm = 0.01%/°C)

Trailing Edge: The portion of the pulse which falls from peak amplitude to zero

Passive Delay Line Test Conditions



- All measurements at 25°C ±5°C
- No loads on taps and output
- 350MHz minimum dual channel oscilloscope on standard models and suitably higher frequency on RCD's specialty Ghz models
- Pulse generator capable of 1nS rise time (or less on specialty types)

- Crystal-based time mark generator
- Input pulse width to be ≥2 x TD
- Input pulse rise = 3nS (10 - 90%)
- Input of delay line under test should see a characteristic impedance near its own
- Output of the delay line under test should be terminated to its characteristic impedance
- Test fixture with massive ground plane
- Duty cycle to be 25% typical
- Typical pulse spacing to be 9 x TD
- Test probe with impedance ≈10x the impedance of the DL under test, stray capacitance <3pF including probe, and inductance <10nH
- Resistors to be non-inductive
- Coax cables shall be used for all equipment interconnects and shall be as short as feasible (18 inches maximum)

Technical Aspects of Active Delay Lines

The combination of a passive delay line with an integrated circuit results in a hybrid Active (Digital) delay line. RCD offers active delay lines in all logic families. The units provide precise delays, and are internally buffered (inputs and outputs) with their respective logic family to minimize reflections. The units feature fast rise time on all outputs. No external components are needed to obtain the specified delay times and performance levels. Considerations common for passive delay lines, such as attenuation, distortion due to tap loading, and distortion due to impedance matching are eliminated.

Standard models feature delay times and performance characteristics optimized for maximum performance/cost ratios. Customized units are also available to meet any particular customer requirement.

Applications

- Timing and pulse synchronization applications in data processing and switching equipment
- Optical Networks
- Microprocessor and memory clock timing generation
- Recovery of asynchronous data signals
- Overcoming timing mismatches
- Skew correction
- Laser and ultrasound control

Active Delay Line Characteristics

The following parameters should be considered by the user to ensure that the optimum delay line is specified for the intended application...

- Logic family
- Delay time and tolerance
- Tap delay time and tolerance
- Package and schematic design
- Input rise time
- Input pulse width
- Duty cycle
- Supply voltage variation
- Output loading
- Temperature coefficient of delay
- Operating and storage temperature
- Special characteristics

Logic Families

RCD offers active delay lines in all standard logic families listed below. Unless indicated otherwise, the information provided in this manual refers to Schottky TTL..

- Schottky TTL (Transistor-Transistor Logic)
- LSTTL (Low Power Schottky TTL)
- ALS (Advanced Low Power Schottky)
- FAST® (Fairchild Advanced Schottky TTL)
- ASTTL (Advanced Schottky)
- 10K ECL (Emitter Coupled Logic)
- 10KH ECL
- 100K ECL
- HCMOS (High Speed CMOS)
- FACT® (Fairchild Advanced CMOS)

Delay Time Measurement, Leading Vs. Trailing Edge

Standard models have the delay times specified and tested at the leading edge only (since the physical switching properties of IC's result in an output pulse width which is typically less than the input pulse width). When both the leading and trailing edge needs to be controlled, specify option "T". It is impossible to achieve an exact match between input and output pulses, however by compensating for the differences in threshold swings, RCD can offer trailing edges which match leading edges within tolerances as tight as 1%. Customized models are also available in which delay times are measured only at the trailing edge.

Rise Time

The output rise times of active delay lines differ from passive types in that they are not dependent on the number of L/C sections, but are instead a function of the integrated circuit utilized in the internal construction.

Depending on the logic family utilized, typical rise times are 1nS to 8nS.

Frequency Response

Rise times are inherent to the logic family utilized, however there are losses resulting from internal circuitry which can have a slight impact on the rise time, and subsequently the bandwidth/ frequency response (refer to Frequency Response section of Passive Delay Lines). The operating frequency level of active delay lines is the minimum pulse width that the delay is guaranteed to pass. A reduction in pulse width below this level would reduce the output widths and degrade the delay accuracy, especially at outputs with higher delay. As a result, customers are recommended to consult with RCD's Engineering Department if the required operating frequency is very close to that of the delay line logic. Samples should be evaluated under actual-use operating conditions to ensure proper performance.

Package and Schematic Design

Active delay lines are available in single, dual, triple, and quadruple delays. Single output delay lines are available with taps to provide five or ten outputs. Programmable delay lines are available in 3, 4, 6, and 8-bit circuits.

RCD's most popular active delay lines are available in 8-pin and 14-pin leaded and gullwing surface mount Dips, 8-Pin Sips, and 14-pin small outline surface mount packages. 16-pin, 18-pin, 24-pin, 32-pin, 48-pin, and 64-pin Dip packages are also utilized on programmable and specialty delay lines.

The most common, and least costly delay line is 14-pin Active TTL, 5-tap model (RCD type A1405), which are generally available from stock. The same unit is available in an auto-insertable package (A1405A) at a slight price premium. Custom schematics are available.

Tap Loading

Tap loading has only a minor impact on active delay lines as long as loading consists of capacitance below 15pF. Trailing edges are generally affected more than leading edges by heavy tap loads. The impact to delay time will typically vary by 1 to 3nS when fully loaded.

Pulse Width

There is generally little or no impact to the delay line if pulse width is at least two times the total delay. As pulse widths become narrower, a degradation to the leading and especially the trailing edges will occur. RCD offers modified designs which utilize specialized internal circuitry to minimize delay variations caused by narrow pulse widths.

Supply Voltage

Unless indicated otherwise on the specific RCD data sheet, a nominal +5VDC ±5% is required for TTL and CMOS logic. ECL uses -5VDC ±5%. 3-volt models are also available. Adequate decoupling should be employed as necessary.

A variation of supply voltage will have a direct impact on delay time. Offsetting the voltage by 5% will typically translate to a 3% variation in delay time.

Duty Cycle

The input pulse repetition rate generally has little or no effect on the performance and accuracy of active delay lines when the duty cycle is less than 25%. Increasing duty cycles affect delay accuracies particularly in regard to trailing edge specifications. RCD offers modified designs which utilize specialized internal circuitry which are less sensitive to duty cycle variation if required.

Combining Active Delay Lines in Series

Cascading of active delay line modules is readily accomplished without additional compensation. Consideration must be given to printed circuit board layout and decoupling procedures, in accordance with the particular logic family utilized.

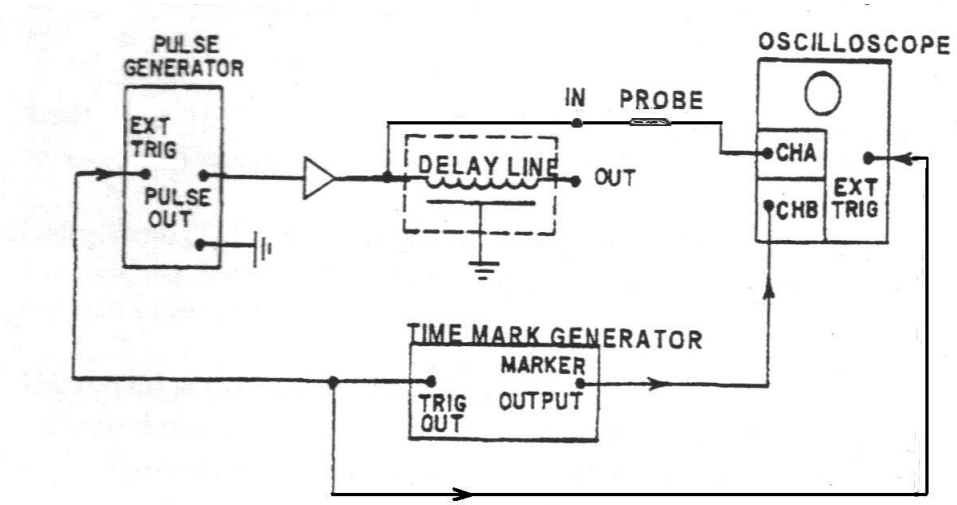
Special Considerations Concerning Short Delay Times

Due to the inherent delay time of the buffer, it may be impossible to achieve first tap delay times below 2nS to 4nS, and therefore time delays shall be measured with respect to the first tap.

ESD Characteristics of Active Delay Lines

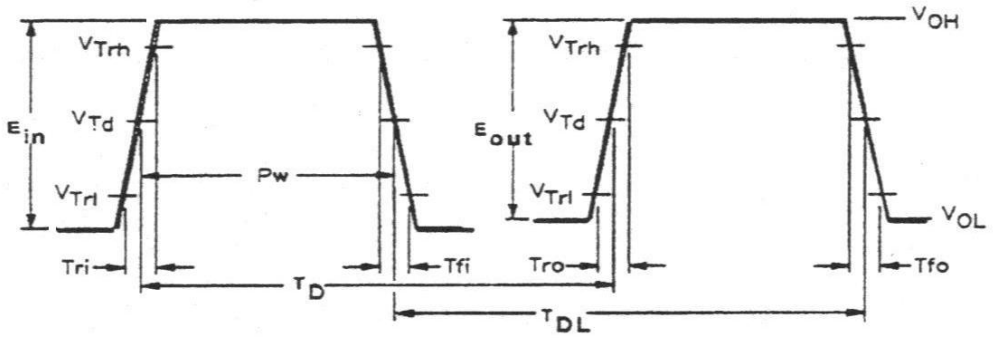
All active delay lines are considered ESD (Electro-Static Discharge) sensitive and therefore users should employ the same handling, packaging, and storage considerations that are utilized on other active components and IC's.

Active Delay Line Test Set-Up (TTL, ECL, CMOS)



- All measurements at 25°C ±5°C
- No loads on taps and output
- 350MHz minimum dual channel oscilloscope
- Pulse generator capable of 2nS rise time
- Crystal-based time mark generator
- Input pulse width to be ≥2 x Total Delay time
- Input pulse rise = 3nS
- Test circuit capacitance <10pF including test probe
- Coax cables shall be used for all equipment interconnects and shall be as short as feasible (18 inches maximum)
- Supply voltage shall be in accordance with the logic family

Active Delay Line Definitions



Input Voltage (E_{in}): The amplitude of the input pulse

Output Voltage (E_{out}): The amplitude of the output pulse

Leading Edge: That portion of the output pulse which rises from V_{OL} to V_{OH}

Trailing Edge: That portion of the output pulse which falls from VOH to VOL (also known as lagging edge)

Delay Time (T_D): The time duration between the VTD voltage point on the leading edge of the input pulse and the VTD voltage point on the leading edge of the output pulse

Trailing Edge Delay Time (T_{DL}): The time duration between the VTD voltage point on the lagging (trailing) edge of the input pulse and the VTD voltage point on the lagging edge of the output pulse

V_{Td} : The specified voltage level at which delay time will be measured as determined by the logic family being used

V_{Trl}: The low voltage reference point for determining the rise time of an active delay line

V_{Trh}: The high voltage reference point for determining the rise time of an active delay line

V_{OL} : The maximum allowable logic"O" output voltage

V_{OH}: The minimum allowable Logic "1" output voltage

Input rise time (T_{ri}): The time duration between the V_{Trl} and the V_{Trh} points on the leading edge of the input pulse

Input fall time (T_{fi}): The time duration between the V_{Trh} and the V_{Trl} points on the trailing edge of the input pulse

Output rise time (T_{ro}): The time duration between the Vtrl and the VTrh points on the leading edge of the output pulse

Output fall time (T_{fo}): The time duration between the V_{Trh} and the V_{trl} points on the trailing edge of the output pulse

Pulse width (P_w): The time duration on the input pulse between the VTD voltage points on the leading and trailing edge of the input pulse

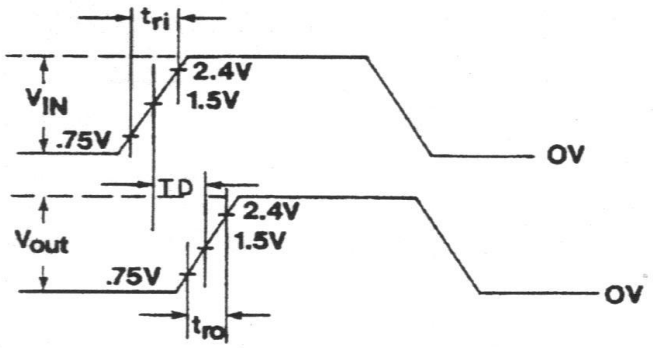
TTL Logic Characteristics

Parameter	Standard Schottky (54S/74S)	Fast Schottky (54F/74F)	Low Power Schottky (54LS/74LS)
+VDC	5.0V	5.0V	5.0V
V_{OH}	3.4V (2.7V min)	3.4V (2.5V min)	3.4V (2.7V min)
E_{In}	3V	3V	3V
V_{Td}	1.5V	1.3V	1.5V
V_{Trl}	0.75V	0.75V	0.75V
V_{Trh}	2.4V	2.4V	2.4V
V_{OL}	0.50V	0.50V	0.50V

ECL & CMOS Logic Characteristics

Parameter	10K ECL	10KH ECL	100K ECL	HCMOS	FACT CMOS
+VDC	0V	0V	0V	5V	5V
-VDC	-5.2V	-5.2V	-4.5V	0V	0V
V_{OH}	-0.98V	-0.98V	-1.025V	4V	3.8V
E_{in}	-.8/-1.8V	-.8/-1.8V	-.8/-1.8V	5.0V	5V
V_{td}	-1.30V	-1.30V	0.5 x Eo	2.5V	2.5V
V_{trl}	0.2 x Eo	0.2 x Eo	0.2 x Eo	0.5V	.5V
V_{trh}	0.8 x Eo	0.8 x Eo	0.8 x Eo	4.5V	4.5V
V_{OL}	-1.63V	-1.63V	-1.62V	0.3V	.44V

TTL Delay Line Waveform

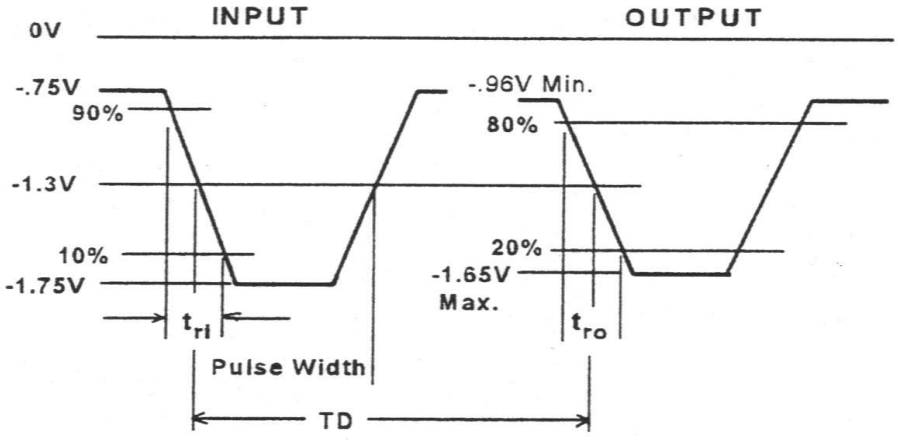


TD = Delay Time: Elapsed time measured between the 1.5V points of the leading edges of the input and output waveforms

t_{ri} = Input Rise Time: Elapsed time measured between the +0.75V and +2.4V points of the leading edge of the waveform

t_{ro} = Output Rise Time: Elapsed time measured between the +0.75V and +2.4V points of the leading edge of the output waveform

ECL Delay Line Waveform



RCD Delay Line Selection Chart

Active, Single Output, Untapped (TTL, CMOS)

RCD Type	Package	Part Number	□ Logic	⊠ Dash Numbers
A01	14-pin Dip, .8" long	A01-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-1000nS 5nS - 1000nS 10nS-1000nS 10nS-1000nS
A01A	Auto-Insertable 14-pin Dip, .8" long	A01A-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-1000nS 5nS - 1000nS 10nS-1000nS 10nS-1000nS
A01S	8-pin Dip, .5" long	A01S-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-500nS 5nS - 500nS 10nS-500nS 10nS-500nS
A01SA	Auto-Insertable 8-pin Dip, .5" long	A01SA-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-500nS 5nS - 500nS 10nS-500nS 10nS-500nS
SA0801	8-pin Sip, .8" long	SA0801-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-500nS 5nS - 500nS 10nS-500nS 10nS-500nS
A01AG	Surface Mount 14-pin Dip, .8" long	A01AG-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-1000nS 5nS - 1000nS 10nS-1000nS 10nS-1000nS
A01SAG	Surface Mount 8-pin Dip, .5" long	A01SAG-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-500nS 5nS - 500nS 10nS-500nS 10nS-500nS

Active, 5 Taps (TTL, CMOS)

RCD type	Package	Part Number	□ Logic	⊠ Total Delay
A1405	14-pin Dip, .8" long	A1405-□- ⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-1000nS 5nS - 1000nS 10nS-1000nS 10nS-1000nS
A1405A	Auto-Insertable 14-pin Dip, .8" long	A1405A-□- ⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-1000nS 5nS - 1000nS 10nS-1000nS 10nS-1000nS
A0805	8-pin Dip, .5" long	A0805-□- ⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-500nS 5nS - 500nS 10nS-500nS 10nS-500nS
A0805A	Auto-Insertable 8-pin Dip, .5" long	A0805A-□- ⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-500nS 5nS - 500nS 10nS-500nS 10nS-500nS
SA0805	8-pin Sip, .8" long	SA0805-□- ⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-500nS 5nS - 500nS 10nS-500nS 10nS-500nS
A0805AG	Surface Mount 8-pin Dip, .5" long	A0805AG-□- ⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-500nS 5nS - 500nS 10nS-500nS 10nS-500nS
A1405AG	Surface Mount 14-pin Dip, .8" long	A1405AG-□- ⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-1000nS 5nS - 1000nS 10nS-1000nS 10nS-1000nS
SMA1405	Surface Mount 14-pin SOIC, 0.5" Long	SMA1405-□- ⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-250nS 5nS - 250nS 10nS-250nS 10nS-250nS

Active, 10 Taps (TTL, CMOS)

RCD Type	Package	Part Number	□ Logic	⊠ Dash No's (Total Delay)
A1410	14-pin Dip, .8" long	A1410-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	20nS-1000nS 10nS -1000nS 20nS-1000nS 20nS-1000nS
A1410A	Auto-Insertable 14-pin Dip, .8" long	A1410A-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-1000nS 20nS-1000nS 10nS -1000nS 20nS-1000nS
SA1410	14-pin Sip, 1.45" long	SA1410-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	20nS-500nS 10nS - 500nS 20nS-500nS 20nS-500nS
A1410AG	Surface Mount 14-pin Dip, .8" long	A1410AG-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	10nS-1000nS 20nS-1000nS 10nS- 1000nS 20nS-1000nS

Active, Dual Independent Delays (TTL, CMOS)

RCD Type	Package	Part Number	□ Logic	⊠ Dash Numbers
A02	14-pin Dip, .8" long	A02□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS
A02A	Auto-Insertable 14-pin Dip, .8" long	A02A□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS
A02S	8-pin Dip, .5" long	A02S-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS
A02SA	Auto-Insertable 8-pin Dip, .5" long	A02SA-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS
A02AG	Surface Mount 14-pin Dip, .8" long	A02AG-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS
A02SAG	Surface Mount 8-pin Dip, .5" long	A02SAG-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS

Active, Triple Independent Delays (TTL, CMOS)

RCD Type	Package	Part Number	□ Logic	⊠ Dash Numbers
A03	14-pin Dip, .8" long	A03-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS
A03A	Auto-Insertable 14-pin Dip, .8" long	A03A-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS
A03S	8-pin Dip, .5" long	A03S-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS
A03SA	Auto-Insertable 8-pin Dip, .5" long	A03SA-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS
A03AG	Surface Mount 14-pin Dip, .8" long	A03AG-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS
A03SAG	Surface Mount 8-pin Dip, .5" long	A03SAG-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS

Active, Quadruple Independent Delays (TTL, CMOS)

RCD Type	Package	Part Number	□ Logic	⊠ Dash Numbers
A04	14-pin Dip, .8" long	A04-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS
A04A	Auto-Insertable 14-pin Dip, .8" long	A04A-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS
A04AG	Surface Mount 14-pin Dip, .8" long	A03AG-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS
A04SAG	Surface Mount 8-pin Dip, .5" long	A03SAG-□-⊠⊠⊠nS	F = Fast TTL H = HCMOS C = FACT Leave blank for std TTL	5nS- 500nS 5nS - 500nS 5nS- 500nS 5nS- 500nS

Active, ECL10K, ECL10KH, ECL100K Logic

RCD Type	Package	Part Number	Logic	⊠ Dash No's (Total Delay)
E105	16-pin Dip, 5-tap, .8" long	E105-⊠⊠⊠nS	ECL 10K	10nS-500nS
E105H	16-pin Dip, 5-tap, .8" long	E105-⊠⊠⊠nS	ECL 10KH	10nS-250nS
E101	16-pin Dip, single output, .8" long	E101-⊠⊠⊠nS	ECL 10K	5nS-500nS
E101H	16-pin Dip, single output,.8" long	E101H-⊠⊠⊠nS	ECL 10KH	5nS-250nS
E102	16-pin Dip, dual output, .8" long	E102-⊠⊠⊠nS	ECL 10K	5nS-100nS
E102H	16-pin Dip, dual output,.8"long	E102-⊠⊠⊠nS	ECL 10KH	5nS-100nS
E103	16-pin Dip, triple output, .8" long	E103-⊠⊠⊠nS	ECL 10K	5nS-100nS
E103H	16-pin Dip, triple output, .8" long	E103H-⊠⊠⊠nS	ECL 10KH	5nS-100nS
E1001	24-pin Dip, single output, 1.3" long	E1001-⊠⊠⊠nS	ECL 100K	5nS-200nS
E1008	24-pin Dip, 8-taps, 1.3"L	E1008-⊠⊠⊠nS	ECL 100K	8nS-200nS
E1004	24-pin Dip, quadruple output. 1.3" L	E1004-⊠⊠⊠nS	ECL 100K	5nS-100nS

Programmable Active Delay Lines (TTL, ECL)

RCD Type	Package	Part Number	□ Logic	⊠ Dash No's Delay/Step
TT3	16-pin Dip, .8" long, 3 Bit	TT3-□-⊠⊠nS	F= Fast TTL Leave blank for std TTL	1nS - 10nS 1nS - 10nS
TT4	32-pin Dip, 1.7" long, 4 Bit	TT4-□-⊠⊠nS	F= Fast TTL Leave blank for std TTL	1nS - 100nS 1nS - 100nS
TT6	48-Pin Dip, 2.5" long, 6 Bit	TT6-□-⊠⊠nS	F= Fast TTL Leave blank for std TTL	1nS - 10nS 1nS - 10nS
TT8	64-Pin Dip, 3.3" long, 8 Bit	TT8-□-⊠⊠nS	F= Fast TTL Leave blank for std TTL	1nS - 5nS 1nS - 5nS
EC3	16-pin Dip, .8" long, 3 Bit	EC3-□-⊠⊠nS	Blank = ECL 10K H = ECL 10KH	1nS - 10nS 1nS - 10nS
EC4	32-pin Dip, 1.7" long, 4 Bit	EC4-□-⊠⊠nS	Blank = ECL 10K H = ECL 10KH	1nS - 10nS 1nS - 10nS
EC6	48-Pin Dip, 2.5" long, 6 Bit	EC6-□-⊠⊠nS	Blank = ECL 10K H = ECL 10KH	1nS - 5nS 1nS - 5nS
EC8	64-Pin Dip, 3.3" long, 8 Bit	EC8-□-⊠⊠nS	Blank = ECL 10K H = ECL 10KH	1nS - 5nS 1nS - 5nS
EC8S	48-Pin Dip, 2.5" long, 8 Bit	EC8S-□-⊠⊠nS	Blank = ECL 10K H = ECL 10KH	.5nS -10nS .5nS - 10nS

Passive Delay Lines, Single Output, Untapped

Type	Package	Total Delay Range	Impedance
P01S	4-pin Dip, .25" long	0.1nS - 1nS	50Ω - 75Ω
P0801	8-pin Dip, .5" long	5nS - 125nS	50Ω - 200Ω
P01	14-pin Dip, .8" long	10nS - 1000nS	50Ω - 500Ω
S01	3-pin Sip, .490" long	1nS - 10nS	500Ω - 200Ω
S02	3-pin Sip, .560" long	1nS - 10nS	50Ω - 200Ω
S03	4-pin Sip,.8"L , P_1 to P_4=.6"	1nS - 100nS	50Ω - 100Ω
S04	4-pin Sip,.8"L , P_1 to P_4=.7"	1nS - 200nS	50Ω - 500Ω
PD1210 (custom)	Surface Mount 1210 Chip 4GHz .125" long	.02nS - .2nS	50Ω
SMP01S	Surface Mount 4-pin Dip, .2" long	0.1nS - 1 nS	50Ω - 75Ω
P0801AG	Surface Mount 8-pin Dip, .5" long	5nS - 125nS	50Ω - 200Ω
P01AG	Surface Mount 14-pin Dip, .8" long	10nS - 1000nS	50Ω - 500Ω

Passive Delay Lines, Tapped

Type	Package	Total Delay Range	Impedance
SP05	5-Tap, 7-pin Sip, .80" long	5nS - 100nS	50Ω - 200Ω
SP10	10-Tap, 14-pin Sip, 1.4" long	10nS - 250nS	50Ω - 200Ω
P0805	5-Tap, 8-pin Dip, .5" long	5nS - 250nS	50Ω - 500Ω
P1410	10-Tap, 14-pin Dip, .8" long	10nS - 1000nS	50Ω - 500Ω
P2420	20-Tap, 24pin Dip, 1.25"long	20nS - 2000nS	50Ω - 500Ω
DL300	20-tap, 24-pin Dip,1.25" long	1000nS - 5000nS	300Ω
DLxxxN	20-tap, 23-pin Dip, 2.4" long	6000nS - 20,000nS	300Ω
P0805-AG	Surface Mount, 5-Tap, 8-pin Dip, .5" long	5nS - 250nS	50Ω - 500Ω
P1410-AG	Surface Mount, 10-Tap, 14-pin Dip, .8" long	10nS - 1000nS	50Ω - 500Ω
P2420G	Surface Mount, 20-Tap, 24pin Dip, 1.25"long	20nS - 2000nS	50Ω - 500Ω

Delay Line Competitor Cross Reference Chart

RCD offers a direct cross to almost every delay line made by other manufacturers. Contact RCD's Sales Department for the latest version of the Delay Line Cross Reference Chart.

RCD Delay Line Questionnaire

Company:_____ Date:_____
Address:_____ Tel: _____
_____ Fax:_____
Name: _____ E-mail:_____ .

RCD offers the widest range of standard and custom delay lines in the industry from 20pS to 20μS including 3V and 5V active (TTL, ECL, CMOS), passive, and programmable models, from DC to 4GHz. If you have a new or existing application and would like assistance selecting the most appropriate delay line, please copy this form , complete the questions, and fax to RCD at (603) 669-5455.

1. Is this an existing____ or new____ application? If existing, what parts are you using now?: Mfr_____ model_____
description_____
Any deficiencies with the existing parts that you'd like RCD to improve upon?_____
If a new application, have you found parts made by any other firm which are working OK?_____ Or which seem promising?_____ If so, please list
Mfr_____ model_____
Desc_____
2. What type of DL is req'd? passive___, active___, either____
3. If passive, please indicate the required rise time or bandwidth_____, and the output impedance_____
4. Logic: TTL____, FastTTL____, ECL10K____, ECL10KH_____ ECL100K____, HCMOS____, FACT_____, other_____
5. Total delay time_____ ±_____%
6. Are taps required?_____ How many?_____ Tap tol: ±____%
7. Package: surface mount is preferred_____ , SM is req'd____, DIP_____ , SIP _____, whichever is most economical_____ . Any special package or size restrictions?_____
8. Please advise quantity level that you'd like quoted (reply required)_____ to _____, target price_____
9. Operating Temp: commercial (0º to 70ºC)____, industrial (-40 to +85ºC)_____, or military (-55 to +125ºC)_____
10. Other requirements (send circuit schematic if helpful):
_____
13. Pin Out (if particular pin out schematic is required describe here):

14. Application Circuit (if applicable,describe application circuit or send circuit diagram):

RCD Components Inc, 520 E.Industrial Pk Dr,Manchester, NH 03109 Tel:(603)669-0054 Fax:(603)669-5455 E-mail: sales@rcdcomponents.com