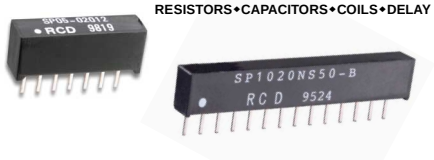
PASSIVE DELAY LINES, TAPPED, SIP PACKAGE

SP05 SERIES - 7 PIN, 5 TAP

SP10 SERIES - 14 PIN, 10 TAP

RoHS Term.W is RoHS compliant

RESISTORS•CAPACITORS•COILS•DELAY LINES



- ❒ Low cost, prompt delivery!
- ❒ Wide variety of values, 5nS to 750nS
- ❒ Fast rise times
- ❒ Detailed application handbook available

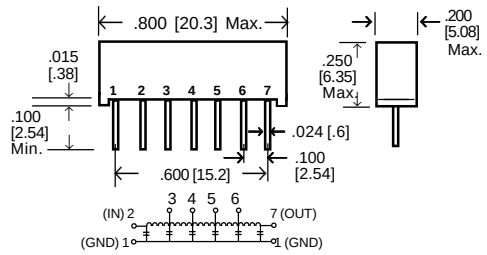
OPTIONS

- ❒ Custom circuits available
- ❒ Non-standard delay times & impedance values
- ❒ Tighter tolerance or temperature coefficient
- ❒ Faster rise times
- ❒ MIL-D-23859 screening
- ❒ Increased operating temperature range

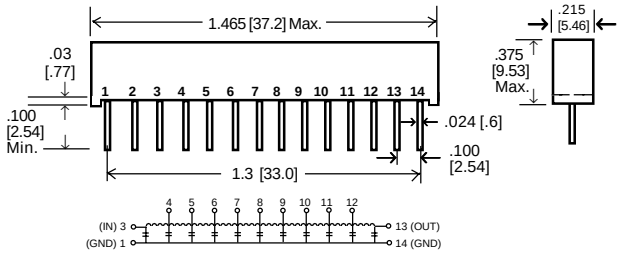
RCD's SP05 and SP10 passive delay line series are a lumped constant design per applicable portions of MIL-D-23859. The units incorporate high performance inductors and multi-layer capacitors, ensuring stable transmission, low temperature coefficient, and excellent environmental performance in space-saving SIP design.

Total Delay Tolerance	±5% or ±0.5nS (whichever is greater)
Tap Delay Tolerance	±5% or ±0.5nS (whichever is greater)
Temperature Coefficient	100ppm/°C Max.
Insulation Resistance	1000MΩ min.
Dielectric Strength	100VDC
Distortion	±10% Max.
Operating Temp. Range	0 to70°C (Opt.39= -40 to 85°C, ER= -55 to125°C)
Operating Freq. (BW)	BW (MHz)=.35/(TR nS x 1000)
Attenuation: (dependent on impedance, low values have lower attenuation)	SP05= 2-5%, SP10=2.5-4% @50Ω, 5-8% @100Ω, 5-10% @200Ω, 5-15% @300Ω, 7-20% @ 500Ω

TYPE SP05 (Available 5nS to 100nS)



TYPE SP10 (Available 10nS to 750nS)



TYPE SP05, 7 PIN 5 TAPS

Total Delay, TD (nS)	Max. Rise Time, TR (nS)	Delay per TAP (nS)	Available Impedance Values (±10%)
5	2.0	1.0 ± .3	50Ω, 100Ω
10	3.3	2.0 ± .4	50Ω, 100Ω
20	6.0	4.0 ± .6	50Ω, 100Ω
25	7.8	5.0 ± 1	50Ω, 100Ω
30	9.0	6.0 ± 1	50Ω, 100Ω
40	12	8 ± 1.5	50Ω, 100Ω
50	15	10 ± 1.8	50Ω, 100Ω
60	18	12 ± 2	50Ω
70	22	14 ± 2	50Ω
75	23	15 ± 3	50Ω
80	24	16 ± 3	50Ω
90	27	18 ± 3	50Ω
100	28	20 ± 3	50Ω

TYPE SP10, 14 PIN 10 TAPS

Total Delay, TD (nS)	Max. Rise Time, TR (nS)	Delay per TAP (nS)	Available Impedance Values (±10%)
10	3	1.0 ± .5	100Ω
20	5.5	2.0 ± .75	50Ω, 100Ω, 200Ω
30	6.5	3.0 ± 1	50Ω, 100Ω, 200Ω
40	8	4.0 ± 2	50Ω, 100Ω, 200Ω, 300Ω
50	10	5.0 ± 2	50Ω, 100Ω, 200Ω, 300Ω, 500Ω
60	12	6.0 ± 2	50Ω, 100Ω, 200Ω, 300Ω, 500Ω
75	15	7.5 ± 2	50Ω, 100Ω, 200Ω, 300Ω, 500Ω
100	20	10 ± 2	50Ω, 100Ω, 200Ω, 300Ω, 500Ω
120	24	12 ± 2	50Ω, 100Ω, 200Ω, 300Ω, 500Ω
150	30	15 ± 2	50Ω, 100Ω, 200Ω, 300Ω, 500Ω
200	40	20 ± 2	50Ω, 100Ω, 200Ω, 300Ω, 500Ω
250	50	25 ± 2	50Ω, 100Ω, 200Ω, 300Ω, 500Ω
300	60	30 ± 2	100Ω, 200Ω, 300Ω, 500Ω 100Ω,
500	100	50 ± 2.5	200Ω, 300Ω, 500Ω
600	120	60 ± 3	300Ω, 500Ω
750	150	75 ± 3.75	300Ω, 500Ω

P/N DESIGNATION:

SP10 ☐ - 10NS - 101 B W

RCD Type

Options: as assigned by RCD (leave blank if std.)

Total Delay

Impedance in 3 digit code: 50R=50Ω, 101=100Ω, 201=200Ω, 301=300Ω, 501=500Ω,

Packaging: B=Bulk

Termination: W= Lead-free, Q= Tin/Lead (leave blank if either is acceptable)

TEST CONDITIONS @25°C

1.) Input test pulse shall have a pulse amplitude of 2.5 volts, rise time of 2nS, and pulse width of 5X total delay.
2.) Delay line to be terminated to within 1% of its charac teristic impedance.
3.) Delay time measured from 50% of input pulse to 50% of output pulse on leading edge with no loads on output.
4.) Rise time measured from 10% to 90% of output pulse.

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