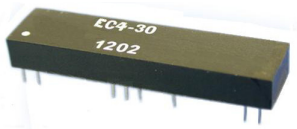
PROGRAMMABLE ECL DELAY LINES

RESISTORS•CAPACITORS•COILS•DELAY LINES

EC4 4 BIT 10K ECL LOGIC

RoHS Term.W is RoHS compliant

- ❒ Delay times from 15nS to 750nS
- ❒ Incremental delays of 1nS to 50nS
- ❒ 32-pin DIP package
- ❒ Mil-spec screening available



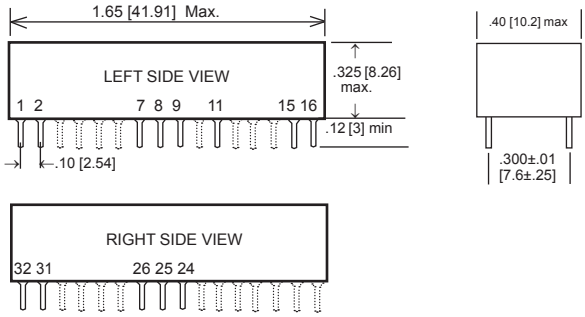
Customized modules can be manufactured to improve accuracies and/or provide customer specified delay times for specific applications.

RCD P/N	Incremental Delay per Step (nS)	Referenced to "0000" - Delay in nS															
		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
EC4-1	1.0 ± .5	0*	1.0	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10	11	12	13	14	15
EC4-2	2.0 ± .5	0*	2.0	4.0	6.0	8.0	10	12	14	16	18	20	22	24	26	28	30
EC4-3	3.0 ± .5	0*	3.0	6.0	9.0	12	15	18	21	24	27	30	33	36	39	42	45
EC4-4	4.0 ± .8	0*	4.0	8.0	12	16	20	24	28	32	36	40	44	48	52	56	60
EC4-5	5.0 ± 1	0*	5.0	10	15	20	25	30	35	40	45	50	55	60	65	70	75
EC4-10	10 ± 1	0*	10	20	30	40	50	60	70	80	90	100	110	120	130	140	150
EC4-20	20 ± 2	0*	20	40	60	80	100	120	140	160	180	200	220	240	260	280	300
EC4-30	30 ± 2.5	0*	30	60	90	120	150	180	210	240	270	300	330	360	390	420	450
EC4-40	40 ± 3	0*	40	80	120	160	200	240	280	320	360	400	440	480	520	560	600
EC4-50	50 ± 3	0*	50	100	150	200	250	300	350	400	450	500	550	600	650	700	750

***** Inherent delay of EC4 10K ECL is 6~10Ns Typ. The initial delay is referenced to setting "0000." For example, the setting "1111" delay of EC4-10 is 150nS ref. to "0000," and 156~160nS typ referenced to the input.

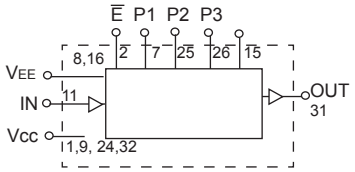
EC4 10K ECL OPERATING SPECIFICATIONS

Logic "1" Input: V_{IH}= -.98V min., I_{IH}= 265µA max
Logic "0" Input: V_{IL}= -1.63V max, I_{IL}= 0.5µA min.
V_{OH} Logic "1" Voltage Out: -.96V min.
V_{OL} Logic "0" Voltage Out: -1.65V max.
Supply Current: 175mA Typ.
Input Pulse Supply Voltage: V_{EE} -5.20VDC, V_{CC} 0VDC
Input Pulse Voltage: 1.0V (-.76V to -1.75V)
Input Pulse Width: 3x Total Delay
Input Pulse Spacing: 10x Total Delay
Input Pulse Rise Time: 2nS (20% to 80%V)
Delay Tolerance: +/-5% or 2nS whichever greater
Operating Temp. Range: 0 to +70°C (specify opt.39 for -40 to +85°C)
Time Delay is measured at 1.3V level, external 100ohm -2VDC
Since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating



Note: Pin #1 is identified via white dot or "1" on top surface

Type EC4 (32-pin DIP package)



CIRCUIT SCHEMATIC: ENABLE input E (pin #2) is active low. Output is disabled (low) when pin #2 is logic high.

*** INPUT LOADING AT PIN #11**: internally connected to ECL gate inputs terminated by Thevenin equivalent of 100 Ohms to -2V.

P/N DESIGNATION: EC4 ☐ - 10 - B W

RCD Type: EC4
Options: assigned by RCD (leave blank if std.)
Delay Time (incremental delay per step)
Packaging: B=Bulk (magazine tube std)
Termination: W=Lead-free, Q=Tin/Lead (leave blank if either is acceptable)

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