

ACTIVE (DIGITAL) DELAY LINES SINGLE, DUAL, TRIPLE, QUAD DELAYS

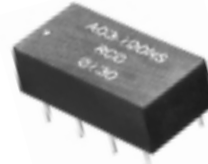
A0 SERIES



Term.W is
RoHS
compliant



RESISTORS•CAPACITORS•COILS•DELAY LINES



- Economical cost, prompt delivery!
- Wide range of values, 5nS to 500nS
- TTL Schottky interfaced

OPTIONS

- Opt.T= trailing edge design
- Opt. F =fast TTL, H =HCMOS, C =FACT
- Opt.A = auto-insertable design
- Opt.39 = -40 to +85°C operating temp.
- Tighter tolerances, faster rise times
- Low power design
- Military screening

STANDARD DELAY TIMES

5nS, 10nS, 15nS, 20nS, 25nS, 50nS,
75nS, 100nS, 250nS, 500nS

Intermediate values available on special order.

SPECIFICATIONS

Operating Temp: 0 to 70°C

Delay Tol: ±2nS or ±5%, whichever greater

Rise Time: 4nS

Peak Soldering Temp: +230°C

CHARACTERISTICS

RCD Type	Independent Delays	Package Style	Circuit
A01	Single	14P	A
A01S	Single	8P	B
A01AG	Single	14SM	A
A01SAG	Single	8SM	B
A02A	Dual	14P	C
A02SA	Dual	8P	D
A02AG	Dual	14SM	C
A02SAG	Dual	8SM	D
A03	Triple	14P	E
A03S	Triple	8P	F
A03AG	Triple	14SM	E
A03SAG	Triple	8SM	F
A04	Quadruple	14P	G
A04AG	Quadruple	14SM	G

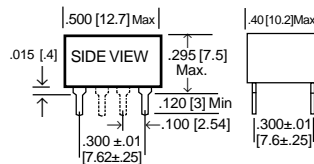
TEST CONDITIONS @25°C

- 1.) Input test pulse voltage: 3.2V
- 2.) Input pulse width: 50nS or 1.2x the total delay (whichever is greater)
- 3.) Input rise time: 2.0nS (0.75V to 2.4V)
- 4.) Delay measured at 1.5V on leading edge only with no loads on output (specify opt. T for trailing edge design)
- 5.) Supply Voltage (Vcc): 5V
- 6.) Pulse spacing: 2x pulse width minimum

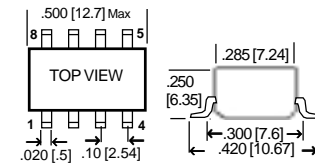
Low cost solution for multiple timing delays in a single package!

RCD's digital delay lines have been designed to provide precise fixed delays with all the necessary drive and pick-off circuitry. All inputs and outputs are Schottky-type and require no additional components to achieve specified delays. Designed to meet the applicable environmental requirements of MIL-D-23859. Type A01 features a single fixed delay, type A02 features two isolated delays, A03 features three delays, and A04 features 4 delays (single delay SIP available). Application Guide available.

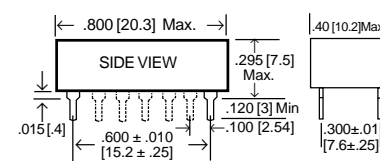
PACKAGE STYLES



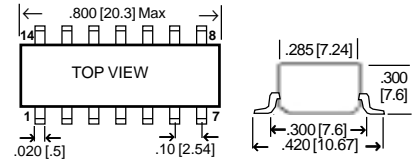
PACKAGE STYLE 8P (8-Pin DIP)



PACKAGE STYLE 8SM (8-Pin SM DIP)

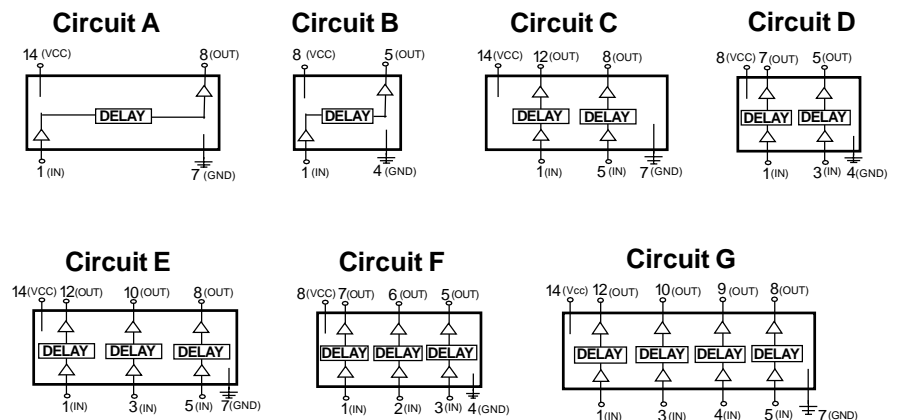


PACKAGE STYLE 14P (14-Pin DIP)



PACKAGE STYLE 14SM (14-Pin SM DIP)

CIRCUIT SCHEMATICS



P/N DESIGNATION:

